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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,594	01/16/2004	Yi-Nan Su	61994.00007	8697

30256 7590 04/20/2005

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EXAMINER	
DANG, TRUNG Q	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 04/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/759,594	SU ET AL.
	Examiner	Art Unit
	Trung Dang	2823

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1, 9, 12, 14, 15, and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee et al. (US 6,607,984).

The rejection is maintained as of record and is repeated herein.

With reference to Figs. 7-12, Lee teaches 18.A method for forming a self

aligned trench isolation, said method comprising:

providing a semiconductor substrate having a pad nitride layer **111** thereon and openings therein, wherein a capacitor is formed in the interior of said opening of said semiconductor substrate;

conformally forming a hard mask layer **124** on said pad nitride layer and said

capacitor (Fig. 8 and col. 6, lines 13-15);

forming a dielectric layer on said hard mask layer (col. 6, lines 29-30 in conjunction with col. 5, lines 12-24);

forming a pattern photoresist layer **130** on said dielectric layer;

removing parts of said dielectric layer, said hard mask layer, said pad nitride layer and said semiconductor substrate, with a part of said dielectric layer as a mask, to form a trench in the middle between partial said two capacitors, wherein a removing rate between said dielectric layer and said hard mask layer is different (Fig. 11 and col. 2, lines 40-42; col. 5, lines 41-43).

Note that, although not shown in Fig. 8, a dielectric layer of SiO_2 is formed

on the bottom antireflecting (BARC) layer **124** (col. 6, lines 29-30 in conjunction with col. 5, lines 12-24) and then the patterned photoresist layer is formed on the SiO_2 dielectric layer. At the step corresponding to the disclosure in col. 6, lines 51-53, the removal of the patterned photoresist layer **130** leaves the SiO_2 dielectric layer intact because the photoresist layer **130** is removed selective to the SiO_2 dielectric layer (col. 5, lines 16-18), and the composite layer of SiO_2 /BARC is used as a mask to etch shallow trench isolation (STI) region **132**.

For claim 9, see col. 5, lines 63-65 for the limitation regarding the buried strap.

For claim 12, Fig. 9 shows the phoresist layer **130** defines an active area (area exposed by the resist) and a device area (area covered by the resist), and the resist mask **130** is aligned with the deep trenches 118.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 2-4, 8, 11, 17-18, 21-22, 24-25, 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al as above in view of Wensley et al. (US 6,566,227).

The rejection is maintained as of record and is repeated herein.

Lee teaches a process as noted above. Lee differs from the claims in not disclosing that the STI region **132** is filled with an isolation comprises an oxide as well as the depths of the deep trench and the shallow trench. Wensley teaches filling STI region with an oxide (col. 6, lines 9-12). Wensley also teaches the depths of the deep trench (DT) and shallow trench (ST) in a DRAM device are about 6 to 10 microns (col. 4, lines 34-35) and about 3,600 Å (col. 5, line 56), respectively. It would have been obvious to one of ordinary skill in the art to modify Lee's process by filling the shallow trench with SiO_2 and forming the DT and ST having depths as noted above because such features are commonly known in the art as shown by Wensley, and the employment of a known practice to make the same would have been within the level of one skilled in the art.

For claims 11,17, 24, and 28 the determination of the thickness of the BARC hard mask layer with respect to the opening and the rate of selectivity between the SiO_2 dielectric layer and the BARC hard mask layer would have been obvious to one having ordinary skill in the art since it has been held that, where the general

conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955). In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990); and In re Geisler, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997).

5. Claims 5-7, 10, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Lee et al. cited above.

The rejection is maintained as of record and is repeated herein.

The admitted prior art depicted in Figs. 1A-1D and described in the pending specification in pages 2-3 teaches substantially the claimed invention, including process steps regarding the forming of the doped buried layer, the diffused lower electrode, and the CMOS transistor fabricated in the device area. The admitted prior differs from the claims in the step of etching STI region **114**, which utilizes a composite hard mask layer comprises a SiO_2 layer formed on a BARC layer as an etch mask to etch the STI region **114**. Lee teaches a process in which a STI region is etched using a composite hard mask layer of SiO_2/BARC as an etch mask for the etching, wherein a removing rate between said SiO2 layer and said BARC layer is different (Fig. 11 and col. 2, lines 40-42; col. 5, lines 41-43). Also see the teaching

of Lee as noted in the above 102 rejection. It would have been obvious to one of ordinary skill in the art to modify the process of the admitted prior art by employing the Lee's technique in the step of forming the STI region **114** because the use of the composite hard mask taught in Lee would provide better lithographic critical dimension control, and hence reducing mask misalignment.

6. Claims 19, 20, 23, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art taken with Lee et al. as applied to claims above, and further in view of Wensley et al. cited above.

The rejection is maintained as of record and is repeated herein.

The combination of the admitted prior art and Lee teaches the process as noted above. The combined process differs from the claims in not disclosing that the STI region **114** is filled with an isolation comprises an oxide. Wensley teaches filling STI region with an oxide (col. 6, lines 9-12). It would have been obvious to one of ordinary skill in the art to modify Lee's process by filling the STI region **114** with SiO_2 because an isolation region formed of SiO2 is commonly practiced in the art as shown by Wensley, and the employment of a known process to make the same would have been within the level of one skilled in the art.

Response to Arguments

7. Applicant's arguments filed 2/03/05 have been fully considered but they are not persuasive.

With respect to Lee's reference, applicants argue that Lee does not disclose a capacitor formed in the opening. The Examiner disagrees. As shown in Fig. 7, storage nodes 118 of the trench capacitor are formed in the opening defined by nitride mask layers 111 and 115. The presence of storage nodes is an indication that capacitors are formed in the trench, and hence in the opening defined by mask layer 111 and 115. Applicants further argue that Lee does not disclose the step of "removing parts of said dielectric layer, said hard mask layer, said pad nitride layer and said semiconductor substrate, with a part of said dielectric layer as a mask, to form a trench in the middle between partial said two capacitors, wherein a different removing rate exists between said insulator layer and said second hard mask layer". The Examiner disagrees. As clearly pointed out in the rejection, although not shown in Fig. 8, a dielectric layer of SiO_2 (corresponding to the claimed insulator layer) is formed on the bottom antireflecting (BARC) layer **124** (col. 6, lines 29-30 in conjunction with col. 5, lines 12-24) and then the patterned photoresist layer is formed on the SiO_2 dielectric layer. At the step corresponding to the disclosure in col. 6, lines 51-53, the removal of the patterned photoresist

layer **130** leaves the SiO_2 dielectric layer intact because the photoresist layer **130** is removed selective to the SiO_2 dielectric layer (col. 5, lines 16-18), and the composite layer of SiO_2 /BARC is used as a mask to etch shallow trench isolation (STI) region **132**. For the etch rate difference between the SiO_2 layer and the BARC layer, see col. 2, lines 40-42. For the limitation regarding a trench formed in the middle between partial said two capacitor, see Fig. 11, wherein trench 132 is formed in the middle between partial two capacitors having storage nodes 118.

With respect to Wensley reference, applicants argue that Wensley does not disclose the part of insulator layer as mask and also does not discloses a different removing rate exists between said insulator layer and said second hard mask layer (BARC layer). The argument is found unpersuasive because the argument was based on the basis of piecemeal analysis of the references. That is, Lee, not Wensley, was used in the rejection to show the aforementioned limitation. However, it is axiomatic that one cannot show nonobviousness by attacking references individually where the rejection, as here, is based on a combination of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

As for the rejection over the admitted prior art in view of Lee (and further in view of Wensley). Again, applicants' arguments are largely directed to what the

cited references teach individually whereas the rejection is based on a combination of references. The arguments are therefore unconvincing for the same reason noted above.

Conclusion

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trung Dang whose telephone number is 571-272-1857. The examiner can normally be reached on Mon-Friday 9:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Trung Dang
Primary Examiner
Art Unit 2823

04/15/05